

WHAT IS CLAIMED IS:

1. A ferro-electric random access memory
comprising:

5 a memory cell having a first ferro-electric
capacitor;

a sense amplifier which determines a data value
of the memory cell by using a reference electric
potential; and

10 a reference electric potential generating circuit
which generates the reference electric potential by
using a paraelectric capacitor and a second ferro-
electric capacitor.

15 2. The ferro-electric random access memory
according to claim 1, wherein one end of the
paraelectric capacitor and one end of the second
ferro-electric capacitor are connected to a common
node, a first driving signal is supplied to the other
end of the paraelectric capacitor, and a second driving
signal is supplied to the other end of the second
20 ferro-electric capacitor.

3. The ferro-electric random access memory
according to claim 2, further comprising:

bit lines; and

25 selective transistors connected between the bit
lines and the common node.

4. The ferro-electric random access memory
according to claim 2, further comprising:

a trimming circuit to finely adjust values of the first and second driving signals.

5 5. The ferro-electric random access memory according to claim 1, wherein the reference electric potential generating circuit is disposed in the memory cell array.

10 6. The ferro-electric random access memory according to claim 1, wherein the reference electric potential generating circuit is disposed at the peripheral portion of the memory cell array.

7. The ferro-electric random access memory according to claim 2, further comprising:

15 a voltage follower circuit which generates a first electric potential having current driving force on the basis of an electric potential of the common node.

8. The ferro-electric random access memory according to claim 7, further comprising:

20 a trimming circuit which generates a second electric potential that finely adjusts a value of the reference electric potential; and

an adder which adds the first and second electric potentials.

9. A ferro-electric random access memory comprising:

25 a memory cell having a first ferro-electric capacitor;

a sense amplifier which determines a data value

of the memory cell by using a reference electric potential;

a reference electric potential generating circuit which generates the reference electric potential by
5 using a second ferro-electric capacitor; and

a trimming circuit which outputs an output electric potential that finely adjusts the value of the reference electric potential.

10. The ferro-electric random access memory
10 according to claim 9, wherein one end of the second ferro-electric capacitor is connected to a common node, and a driving signal is supplied to the other end of the second ferro-electric capacitor.

11. The ferro-electric random access memory
15 according to claim 10, further comprising:

bit lines; and

selective transistors connected between the bit lines and the common node.

12. The ferro-electric random access memory
20 according to claim 9, wherein the trimming circuit includes a component by a paraelectric capacitor, and finely adjusts the value of the reference electric potential in consideration of the component.

13. The ferro-electric random access memory
25 according to claim 9, wherein the reference electric potential generating circuit is disposed in the memory cell array.

14. The ferro-electric random access memory according to claim 9, wherein the reference electric potential generating circuit is disposed at the peripheral portion of the memory cell array.

5 15. The ferro-electric random access memory according to claim 10, further comprising:

 a voltage follower circuit which outputs an output electric potential having current driving force on the basis of an electric potential of the common node.

10 16. The ferro-electric random access memory according to claim 15, further comprising:

 an adder which adds the output electric potential of the trimming circuit and the output electric potential of the voltage follower circuit.

15 17. A read method of a ferro-electric random access memory, comprising:

 pre-charging first and second bit lines when data is read from a memory cell having a first ferro-electric capacitor;

20 changing an electric potential of the first bit line in accordance with a value of the data;

 generating a reference electric potential by using a paraelectric capacitor and a second electric capacitor;

25 setting an electric potential of the second bit line to the reference electric potential; and

 determining the value of the data on the basis of

a potential difference between the first and the second bit lines.

18. The read method according to claim 17, wherein the reference electric potential is generated due to
5 a first driving signal being supplied to the other end of the paraelectric capacitor, and a second driving signal being supplied to the other end of the second ferro-electric capacitor.

19. The read method according to claim 18, wherein
10 values of the first and second driving signals are finely adjusted by a trimming circuit.

20. The read method according to claim 17, wherein the reference electric potential becomes an electric potential having current driving force by a voltage
15 follower circuit.

21. The read method according to claim 20, wherein the value of the reference electric potential is finely adjusted by a trimming circuit.